## CLAIMS

1. A phase difference detector adapted to generate a phase difference signal indicative of a phase difference between a first signal and a second signal, comprising:

a first bistable element clocked by the first signal and having a first output signal;

a second bistable element clocked by the second signal and having a second output signal;

means for determining the change of said phase difference signal, responsive to said first and second output signals, and

a reset circuit having a first and a second inputs respectively connected to said first and second output signals and adapted to determine the resetting of the first and the second bistable elements responsive to the attainment of a respective prescribed state on the part of the first and the second output signals,

said first and second inputs of the reset circuit substantially symmetrical to each other from the point of view of a respective input impedance associated with each of them.

2. The phase difference detector of claim 1, in which the reset circuit includes, associated with said first and second inputs, input impedance symmetrization means.

3. The phase difference detector of claim 2, in which the reset circuit includes a logic circuit with a first logic input and a second logic input, respectively coupled to the first and the second signals and adapted to detect the attainment of the respective prescribed state by the first and the second output signals, and in which said symmetrization means are associated with said first and second logic inputs.

4. The phase difference detector of claim 3, in which said symmetrization means include decoupling means of the first and second inputs of the reset circuit from the first and second logic inputs, respectively.

5. A phase-locked loop circuit adapted to generate an output signal locked in frequency and phase to a reference signal, comprising:

a phase difference detector adapted to detect a phase difference between the reference signal and a signal derived from the output signal, and an oscillator controlled by a phase difference signal generated by the phase difference detector, characterized in that the phase difference detector is realized according to claim 1.

6. The phase-locked loop circuit of claim 5, comprising a frequency divider adapted to generate the derived signal through division in frequency of the output signal, said divider being controlled to implement a division factor equal to an integer number.

7. The phase-locked loop circuit of claim 5, comprising a frequency divider adapted to generate the derived signal through division in frequency of the output signal, said divider being controlled to implement an average division factor equal to a non-integer number.

8. A frequency synthesizer circuit, comprising a reference signal generator and a phase-locked loop circuit realized according to claim 5.

9. A method for improving the linearity characteristics of the response of a phase difference detector adapted to generate a signal indicative of a phase difference between a first signal and a second signal, the phase detector having a first bistable element clocked by the first signal and having a first output signal, a second bistable element clocked by the second signal and having a second output signal,

means for determining the variation of said signal indicative of the phase difference, responsive to said first and second output signals, and a reset circuit having a first and a second inputs respectively connected to the said first and second output signals and adapted to determine the resetting of the first and second bistable elements in response to the attainment of a respective prescribed state by the first and the second output signals, the method comprising:

making said first and second inputs of the reset circuit substantially symmetrical to each other from the point of view of an input impedance associated to each one of them.

10. A phase difference detector comprising:

a first logic element having an input terminal coupled to receive a first clock signal; and having an output terminal;

a second logic element having an input terminal coupled to receive a second clock signal and having an output terminal;

a feedback circuit having two inputs and an output, a first input being coupled to the output terminal of the first logic element and a second input coupled to the output of the second logic circuit;

a feedback line coupled from the output of the feedback circuit to a control input terminal in each of the first and second logic elements; and

a phase correction circuit coupled to the output of the first logic element and to the output of the second logic element and providing at its output a phase correction signal.

11. The circuit according to claim 10 wherein the feedback circuit includes a delay circuit that provides a timed delay from the outputs to the control inputs of the first and second logic elements.

12. The circuit according to claim 11 wherein the control input terminal is a feed back terminal.

13. The circuit according to claim 10 wherein the feedback circuit further includes a logic gate coupled to the first and second outputs from the first and second logic elements and outputs a signal to the delay circuit.

14. The circuit according to claim 13 further including:

a symmetrization element coupled to the first and second outputs of the first and second logic elements.

15. The circuit according to claim 14 wherein the symmetrization element includes two transistors having control terminals coupled to the respective first and second output terminals of the first and second logic elements.